SY89859U

Precision Low-Power 8:1 MUX with Internal Termination and 1:2 LVPECL Fanout Buffer

General Description

The SY89859U is a low jitter, low-power, high-speed 8:1 multiplexer with a 1:2 differential fanout buffer optimized for precision telecom and enterprise server distribution applications. The SY89859U distributes clock frequencies from DC to >2.5GHz, and data rates to 2.5Gbps guaranteed over temperature and voltage.

The SY89859U differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV (200mVpp) without level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100K-compatible LVPECL with extremely fast rise/fall time guaranteed to be less than 180ps.

The SY89859U features a patent-pending isolation design that significantly improves on channel-to-channel crosstalk-induced jitter performance.

The SY89859U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89859U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.



Precision Edge®

Features

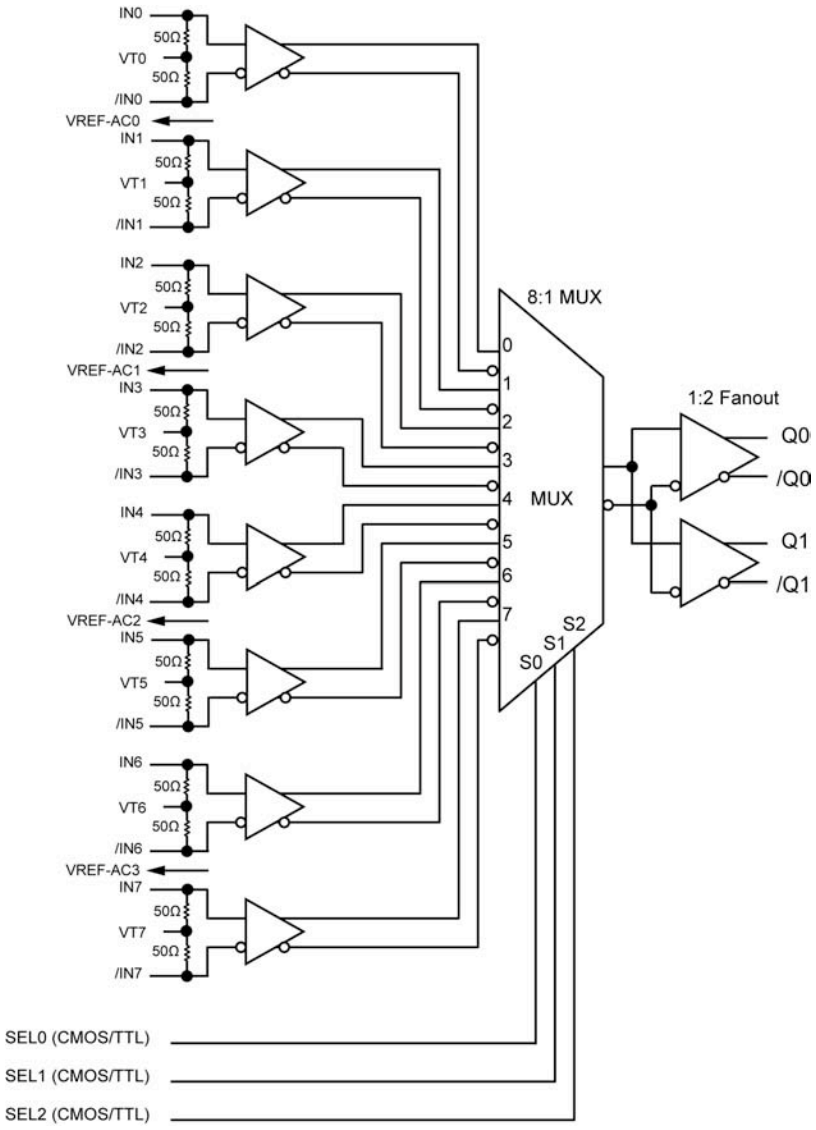
- Selects between 1 of 8 inputs, and provides 2 precision, low skew 100K-compatible LVPECL output copies
- Low power: 150mW typ. (2.5V)
- Guaranteed AC performance over temperature and voltage:
  - DC to >2.5Gbps
  - DC to >2.5GHz
  - <690ps propagation delay
  - <180ps t_r/t_f time
  - <20ps skew (output-to-output)
- Unique, patent-pending channel-to-channel isolation design provides superior crosstalk performance
- Ultra-low jitter design:
  - <1ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
  - <10ps$_{PP}$ total jitter (clock)
  - <1ps$_{RMS}$ cycle-to-cycle jitter
  - <0.7ps$_{RMS}$ crosstalk-induced jitter
- Unique, patented input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C industrial temperature range
- Available in 44-pin (7mm x 7mm) MLF® package

Applications

- Data communication systems
- All SONET/SDH data/clock applications
- All Fibre Channel applications
- All Gigabit Ethernet applications

Precision Edge is a registered trademark of Micrel, Inc.
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology.

Functional Block Diagram



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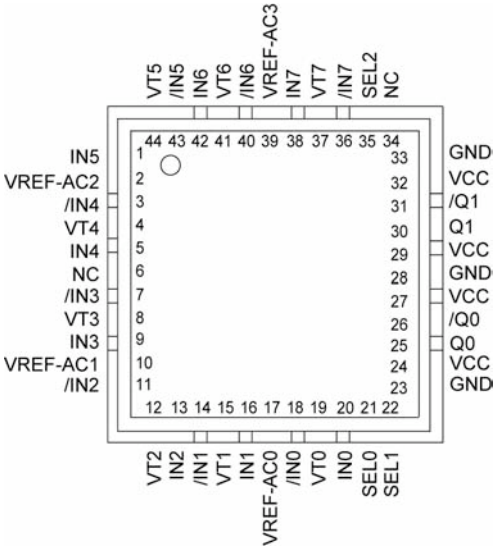
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89859UMG	MLF-44	Industrial	SY89859U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89859UMGTR[2]	MLF-44	Industrial	SY89859U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



44-Pin MLF® (MLF-44)

Truth Table

SEL2	SEL1	SEL0	Q	/Q
L	L	L	IN0	/IN0
L	L	H	IN1	/IN1
L	H	L	IN2	/IN2
L	H	H	IN3	/IN3
H	L	L	IN4	/IN4
H	L	H	IN5	/IN5
H	H	L	IN6	/IN6
H	H	H	IN7	/IN7

Pin Description

Pin Number	Pin Name	Pin Function
20, 18 16, 14 13, 11 9, 7 5, 3 1, 43 42, 40 38, 36	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3 IN4, /IN4 IN5, /IN5 IN6, /IN6 IN7, /IN7	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV (200mVpp). Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
19, 15 12, 8 4, 44 41, 37	VT0, VT1 VT2, VT3 VT4, VT5 VT6, VT7	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details. For a CML or LVDS inputs, the VT pin is left floating.
17 10 2 39	VREF-AC0 VREF-AC1 VREF-AC2 VREF-AC3	Reference Voltage: These outputs bias to V_{CC}–1.2V. They are used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF-AC to the VT pin and bypass with a 0.01µF low ESR capacitor to VCC. See “Input Interface Applications” section for more details.
21 22 35	SEL0 SEL1 SEL2	The single-ended TTL/CMOS-compatible inputs select the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. The threshold voltage is $V_{TH} = V_{CC}/2$.
24, 27, 29, 32	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitors and place as close to each VCC pin as possible.
25, 26 30, 31	Q0, /Q0 Q1, /Q1	Differential Outputs: These 100K-compatible LVPECL output pairs are the outputs of the device. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC}–2V.
23, 28, 33	GND Exposed Pad	Ground. GND and exposed pad must both be connected to the same ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage
  SEL0, SEL1, SEL2 ..... –0.5V to V_{CC}
  IN0, /IN0, IN1, /IN1,…/IN7, /IN7 ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
Termination Current
  Source or sink current
  VT0, VT1, VT2,…VT7 ..... ±100mA
Input Current
  Source or sink current
  IN0, /IN0, IN1, /IN1,…IN7, /IN7 ..... ±50mA
VREF Output Current
  VREF-AC0, VREF-AC1…, VREF-AC3 ..... ±2mA
Lead Temperature (soldering, 20 sec.) .....+260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  MLF® (θ_{JA})
    Still-Air ..... 24°C/W
  MLF® (ψ_{JB})
    Junction-to-Board ..... 12°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		60	85	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 5	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-to-/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

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100K LVPECL Output DC Electrical Characteristics[6]

V_{CC} = +2.5V ±5% or 3.3V ±10%, R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage (Q, /Q)		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Differential Swing	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = +2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	I_{IH} @ V_{IN} = V_{CC}	–125		40	µA
I_{IL}	Input LOW Current	I_{IL} @ V_{IN} = 0.5V	–300			µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or 3.3V ±10%; V_{IN} ≥100mV (200mVpp); R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency		2.5			Gbps
			2.5	3.5		GHz
t_{pd}	Differential Propagation Delay					
	IN-to-Q		360	475	640	ps
	SEL-to-Q		200	600	850	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient	IN-to-Q		300		fs/°C
		SEL-to-Q		400		
t_{SKEW}	Output-to-Output Skew	Note 8	5		20	ps
	Part-to-Part Skew	Note 9			200	ps
t_{JITTER}	Data					
	Random Jitter (RJ)	Note 10			1	ps_{RMS}
	Deterministic Jitter (DJ)	Note 11			10	ps_{PP}
	Clock					
	Cycle-to-Cycle Jitter	Note 12			1	ps_{RMS}
	Total Jitter (TJ)	Note 13			10	ps_{PP}
	Adjacent Channel Crosstalk-induced Jitter	Note 14			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	50	110	180	ps

Notes:

7. High-frequency AC-parameters are guaranteed by design and characterization.
8. Output-to-output skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Random jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
11. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
14. Crosstalk-induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar, differential clock frequencies that are asynchronous with respect to each other at the inputs.

Single-Ended and Differential Swings

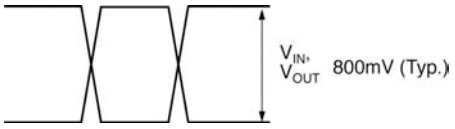


Figure 1a. Single-Ended Voltage Swing

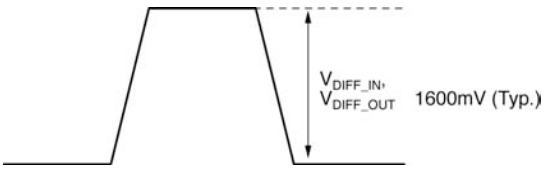
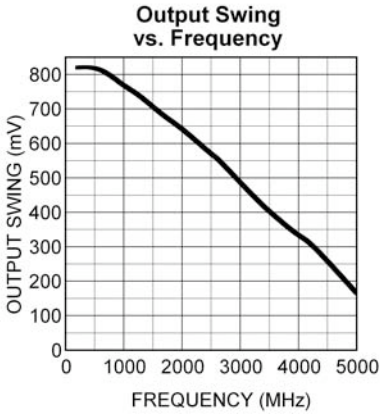


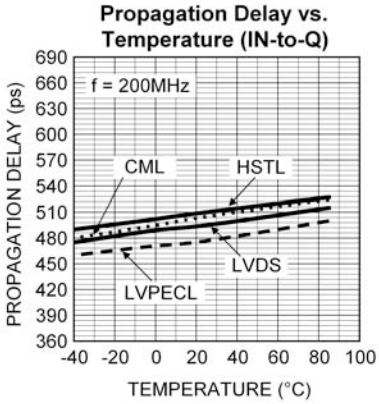
Figure 1b. Differential Voltage Swing

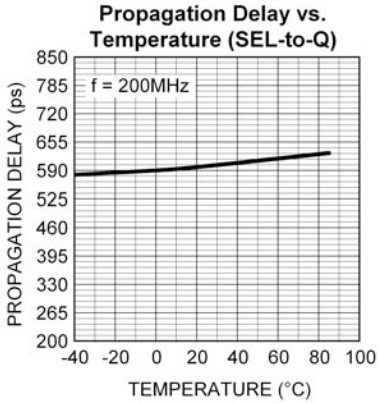
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Typical Operating Characteristics

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV (200mVpp), R_L = 50Ω to V_{CC}–2V; T_A = 25°C, unless otherwise stated.



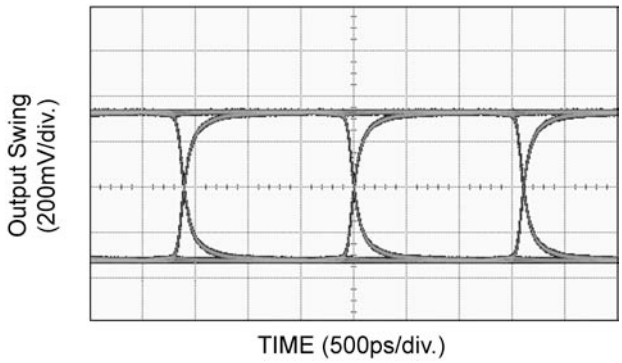




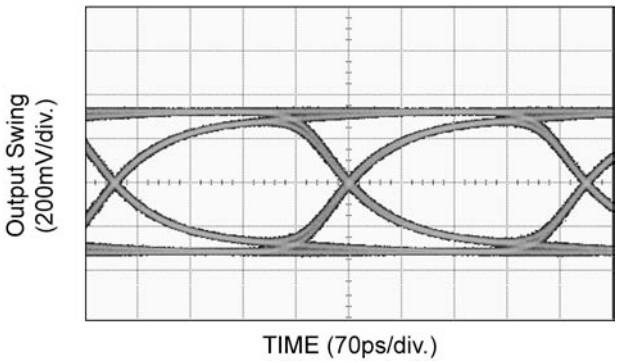
Functional Characteristics

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV (200mVpp), R_L = 50Ω to V_{CC}–2V; T_A = 25°C, unless otherwise stated.

622Mbps Output



3.2Gbps Output



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Input and Output Stages

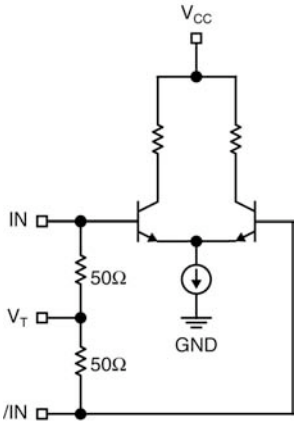


Figure 2a. Simplified Differential Input Stage

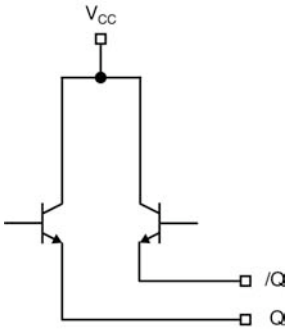


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

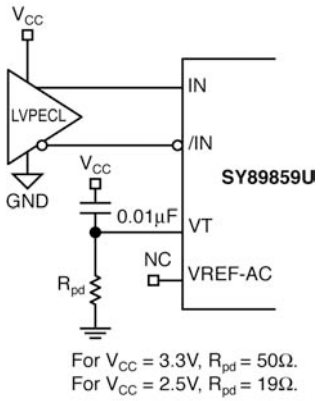


Figure 3a. LVPECL Interface (DC-Coupled)

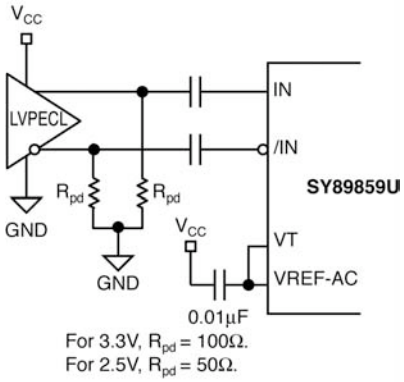
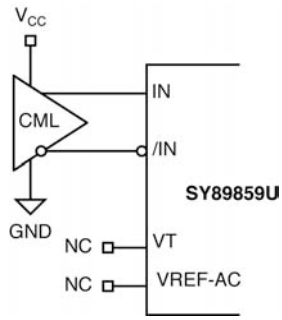


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

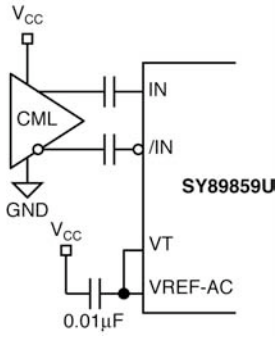


Figure 3d. CML Interface (AC-Coupled)

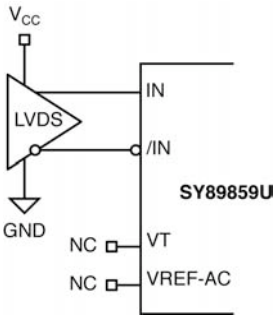


Figure 3e. LVDS Interface

LVPECL Output Interface Applications

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing which result in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output including: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-Resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

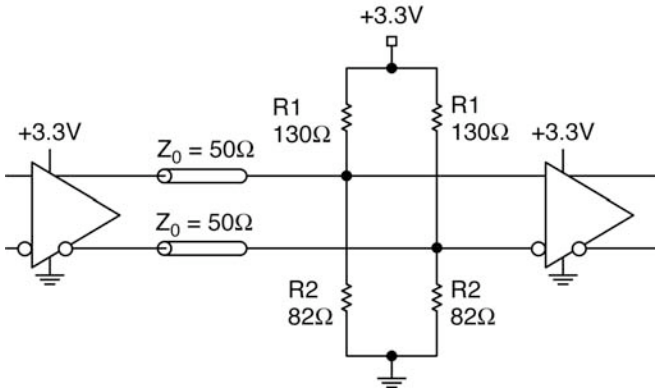


Figure 4a. Parallel Thevenin-Equivalent Termination

Note:

For 2.5V system, R1 = 250Ω, R2 = 62.5Ω.

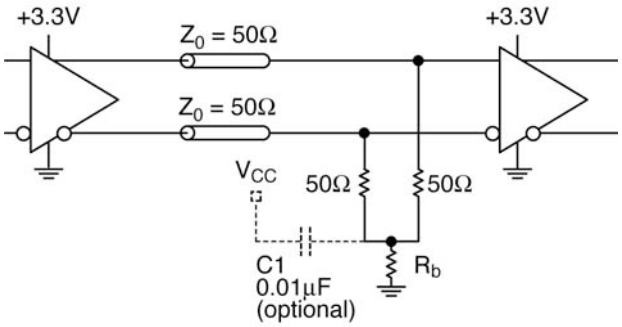


Figure 4b. Parallel Termination (3-Resistor)

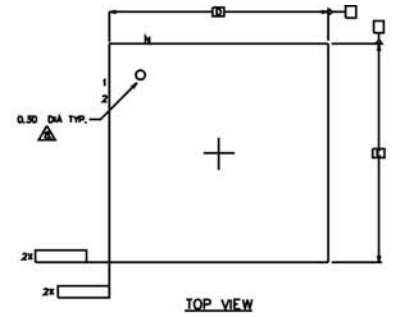
Note:

For 2.5V system, Rb = 19Ω.

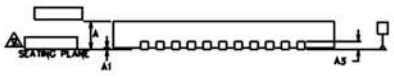
Related Product and Support Documentation

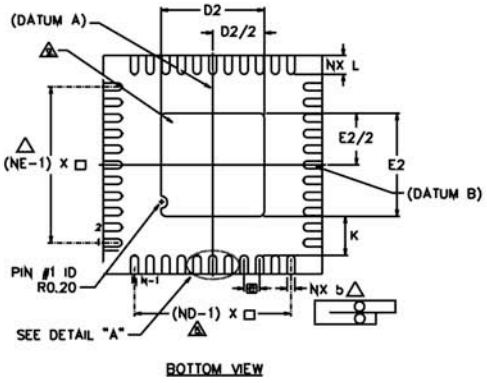
Part Number	Function	Data Sheet Link
SY58037U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 CML Fanout Buffer	http://www.micrel.com/product-info/products/sy58037u.shtml
SY58038U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 LVPECL Fanout Buffer	http://www.micrel.com/product-info/products/sy58038u.shtml
SY58039U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 400mV LVPECL Fanout Buffer	http://www.micrel.com/product-info/products/sy58039u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf

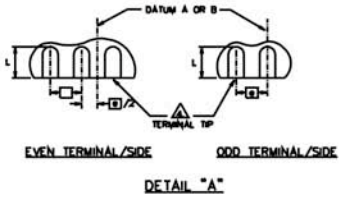
Package Information



NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220

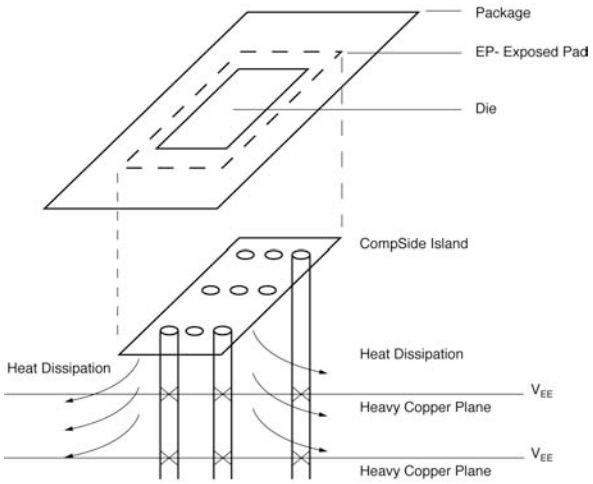






SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		5
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	—	12	2

44-Pin MLF® (MLF-44)



PCB Thermal Consideration for 44-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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